WLCSP AND FLIP CHIP BUMPING TECHNOLOGIES

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ABSTRACT

WLCSP bumps have traditionally been produced by dropping preformed solder spheres through a metal template onto silicon wafers using modified surface mount stencil printers [1]. The squeegee blades associated with these printers have been retrofitted with a special fixture in which spheres are gravity feed down through a narrow slot. This same stencil printer is often used to apply the flux to the wafer just prior to sphere dropping. This technique is applicable for many applications but there are several issues are associated with this technology that limit its widespread use in high volume and high yield applications. These limitations include: 1) there is a practical lower limit to the size of sphere that can be dropped, 2) the seal between the slotted fixturing and the wafer can fail, causing a release of all the spheres into the tool (often referred to as bursts or escapes), and 3) the yields are statistically low.

Flip Chip bumps have traditionally been produced by electroplating or paste printing processes. Both technologies have been implemented in high volumes for PdSn bumping at many facility across the world. The electroplating technique is somewhat limited for use in smaller facilities due to the high capital and operation costs. In addition, ternary alloys, like SnAgCu are difficult to plate with consistent results. There is also a practical upper limit to the size of the bump that can be produced, and most applications rare for fine pitch bumping.. The paste printing technologies are very versatile with respect to the alloy composition that can be use, but is limited to pitches around 200μm for 100 μm tall bumps.

One new WLCSP technology that is showing high promise toward eliminating these limnitations for both WLCSp and Flip Chip, is Wafer Level Solder Sphere Transfer (also called Gang Ball Placement) [2]. This technology uses a patterned vacuum plate to simultaneous pick up all of the preformed solder spheres, optically inspect for yield, and then transfer them over to the wafer. This paper will discuss this technology and the process parameters for producing WLCSP bumps. Throughput levels of 25 to 30 wafers per hour were measured. Yield losses of less than 10ppm were realized for placing 300 μm spheres onto 200mm wafers with ~80,000 I/Os. Similar yields have been observed for placing 60μm flip chip sized spheres onto semiconductor wafers.

Keywords: WLCSP, Flip Chip, Solder Sphere, Gang Ball Placement, Electroless Nickel, Solder Ball Transfer.

INTRODUCTION

Wafer bumping is often separated into two different categories: flip chip bumping (FC) and wafer level chip scale packaging (WLCSP). This categorization and affiliated nomenclature is partially based on the solder bump size and the type of equipment used to create the bump.

"Flip Chip" refers to bumps on semiconductor wafers which are in the range of 50 to 200 μm in height. "WLCSP" refers to bumps that are in the range of 200 to 500 μm in height. Flip Chip bumps are traditionally created by electroplating, evaporation (C4), or paste printing; [3] while WLCSP bumps are mainly produced by dropping preformed solder spheres onto the wafer.

Pushing the limits of each of these technologies has allowed some overlap between these two bumping classifications. But for the most part, volume manufacturing of flip chip bumps and WLCSP bumps are carried out using different processes steps and different types of equipment. One new technology that is showing high promise toward completely bridging this technology gap is Wafer Level Solder Sphere Transfer (WLSST).

WLSST technology uses a patterned vacuum tooling fixture to simultaneously pick up preformed spheres and transfer them all over to the wafer at once. Figure 1 outlines the basic steps in the transfer process. First, a tooling plate (vacuum stencil) is lowered into the sphere reservoir. Vacuum is applied to the tooling plate to selectively pick up the spheres. This fixture is then inspected for missing or extra spheres. The tooling is then aligned to the wafer and

lowered to bring the solder spheres into contact with the wafer pads. Finally, the vacuum is turned off; the tooling plate is raised; and the solder spheres are reflowed.

The tooling plate is patterned with openings that correspond directly with the location of the I/O pads on the wafer. This tooling is created using similar methods to that of making a nickel plated surface-mount stencil. The size of openings in the tooling is designed to be slightly smaller than the size of spheres that will be placed onto the wafer. Because this tooling plate can be made with such accuracy and because the WLSST equipment has a placement accuracy of better than ±15µm, the process can be used for both WLCSP and flip chip applications.

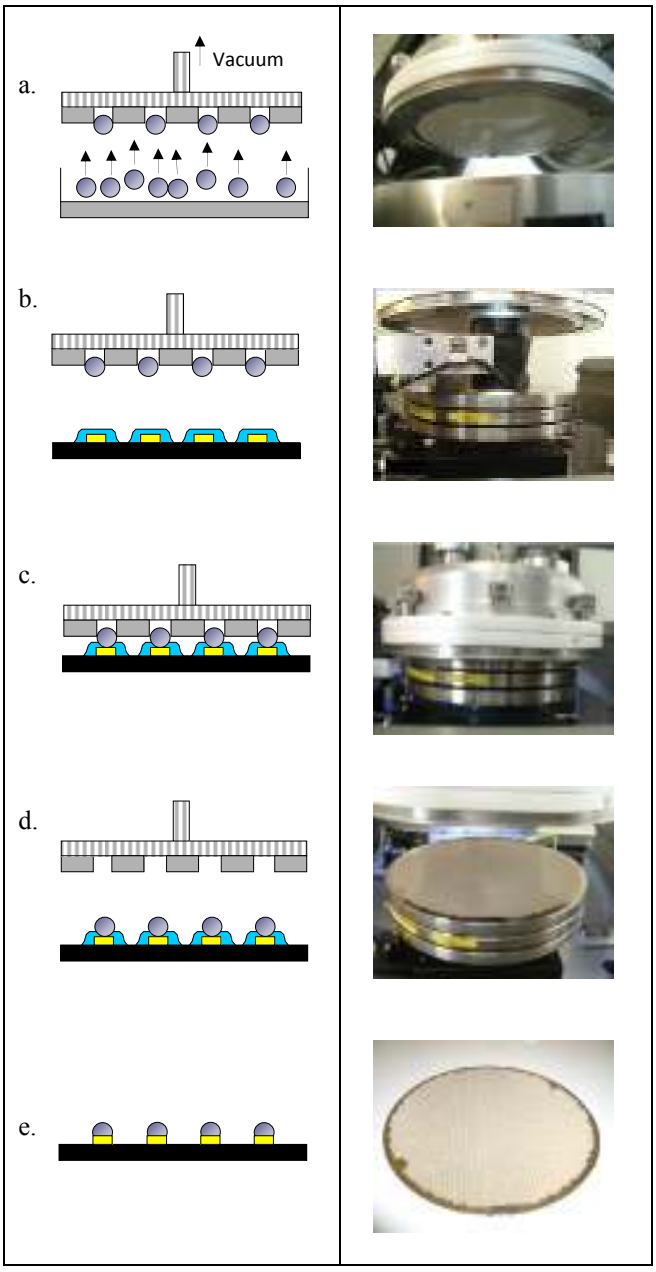

Figure 1. Wafer Level Solder Sphere Transfer (WLSST) Process Flow.

a. **Pick Up Spheres:** Lower vacuum tooling head into sphere reservoir and apply vacuum to tooling,
b. **Inspect and Align:** Inspect for missing spheres and align to wafer (a pre-fluxed wafer is automatically placed onto the wafer chuck just prior to each solder sphere transfer operation),
c. **Mate Spheres to Wafer:** Lower tooling head and bring spheres into contact with the fluxed wafer pads,
d. **Raise Tooling Head:** Turn off vacuum and raise vacuum tooling,
e. **Remove Wafer and Reflow:** Automatically transfer wafer to reflow station.

PROCESS INTEGRATION

When choosing one the various bumping technologies (process flow and equipment) for creating solder bumps for either Flip Chip or for WLCSP applications, there are several operations in addition to the solder deposition process that should be considered. These include under-bump-metallurgy (UBM), fluxing, reflow, rework, cleaning, and inspection. For most of the traditional bumping technologies, these are discrete operations and therefore require distinct and separate tools for each process step. The Wafer Level Solder Sphere Transfer tool combines several of these operations into a single tool and that can lead to higher throughput, higher yields, and lower costs.

The Under-Bump-Metallurgy (UBM) is an integral part of all bumping processes. Both aluminum-based and copper-based integrated circuits (ICs) require some interfacial material between the I/O pad and the solder bump. This material is typically deposited by physical vapor deposition (PVD) [4], electroplating [5], or electroless plating [6]. All three of these UBM technologies are compatible with the Wafer Level Solder Sphere Transfer bumping technology and are carried out as separate steps prior to the actual solder bumping operation. The choice between these three UBM technologies is often dictated by cost and reliability. PVD and electroplating techniques require both high vacuum and photolithography steps and are therefore considered high cost operations. The electroless nickel/gold process technology is a simple wet chemical process that is self-patterning and is therefore low cost in relations to its total capital investment and operational costs [7]. The electroless nickel process is continuing to make inroads into the bumping industry, not only because of its low cost, but also because of its high throughput and versatility (plating on either copper or aluminum based semiconductors). Recently, the electroless nickel/gold process has been shown to have the addition advantage over the other UBM technologies in both mechanical and thermal reliability [8]. The intermetallics formed between the solder and the electroless nickel has surpassed both the sputtered and

electroplated technologies in mechanical testing, (drop testing, high-speed shear, and high-speed pull), thermal cycling, and humidity testing.

The electroless nickel process is a maskless process that uses wet chemical techniques to selectively create layers of nickel and gold on the I/O pads of semiconductor wafers. For aluminum based integrated circuits [9], the chemical sequence is to first clean off the pads of any organic or silicon based contaminates which may occur due to wafer handling, storage, or variations in the manufacturing process. The second step is to remove any native oxide that may have built up on the aluminum pad surface. This is typically performed using caustic based etching chemicals. The next step is to activate the surface of the aluminum. The most commonly used wet chemical system for this is "zincation", where a zinc oxide solution is used to replace some of the pad aluminum with zinc in an electrochemical reaction. Empirical research has shown that by stripping this zinc layer off and then reforming it in a second zincation step, one creates a higher quality layer of zinc. This is often referred to as "double zincation". This zinc layer changes the electric potential of the aluminum pad, and when immersed in a nickel sulfate solution, nickel replaces this zinc and an autocatalytic nickel reaction continues. By adjusting the time, temperature, pH, and chemical concentrations of the nickel plating bath, one can create nickel structures between 1 and 25 microns tall.

For most applications the deposition of solder does not immediately follow the nickel deposition process. The nickel surface will oxidize fairly quickly, and therefore a thin layer of a noble metal is typically deposited on top of the nickel to protect the surface from oxidation. There are two common metals (Pd and Au) which are compatible with the electroless nickel process and can be deposited sequentially within the same plating line using either immersion or electroless based processes.

1) Pad Cleaning
2) Aluminum Etch
3) Zincation I
4) Zinc Stripping
5) Zincation II
6) Nickel Plating
7) Gold and/or Palladium Plating

For copper based semiconductors [10], the nickel and gold plating baths are the same as those for aluminum based semiconductors. Several acid base cleaning steps are typically used to clean off contaminates and to remove copper oxide from the surface of the I/O pads. The activation step for copper is similar to that used in the laminate board plating industry, and usually uses a palladium based catalyst. The know-how for plating Cu semiconductors is the ability to selectively catalyze the copper I/O pads without activating the surrounding passivation [11]. Figure 2 shows a typical electroless nickel and immersion gold plating line.

1) Pad Clean
2) Copper Etch
3) Catalytic Activation
4) Nickel Plate
5) Gold and/of Palladium Plate

Figure 2. Electroless Nickel Plating Line (Pac Tech PacLine 300 A50).

The nickel thickness required for solder based bumping applications is typically between 3 and 5 microns. This selection of nickel thickness is partially based on historical thicknesses, which for the most part was arbitrary, but recent reliability testing has confirmed that electroless nickel layers in this thickness range create highly reliable structures. Figures 3 shows a top down SEM view of an electroless nickel/gold plated pad on a silicon wafer.

Figure 3. Top View of an Aluminum Bond Pad (left), and Electroless Nickel/Gold Plated Bond Pad (right).

Several of the remaining six process steps (fluxing, solder deposition, rework, reflow, inspection, and cleaning) can be carried out independently or as part of the Wafer Level Solder Sphere Transfer tool (see Figure 4). The WLSST equipment can be configured in several different ways to match the predominant bump size, preferred fluxing technique, and inspection criteria; with other processes and equipment in the fab. For example, the flux can be applied prior to sphere placement by either screen-printing, stencil printing, spin coating; or the Wafer Level Solder Sphere Transfer tool itself can be configured with a flux coating

station to increase throughput. The tool can also be fitted with a hot plate reflow station, inspection capabilities, and a bump rework station (laser based solder jet [12].

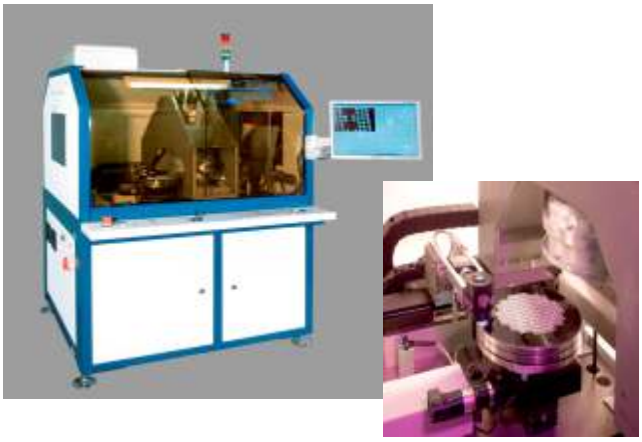

Figure 4. Images of the Wafer Level Solder Sphere Transfer Tool (Pac Tech Ultra-SB^2 or GBP).

Even though the Wafer Level Solder Sphere Transfer tool can perform both flip chip bumping and WLCSP bumping operations. The configuration of the tool is often dictated by the product distribution (flip chip vs WLCSP volumes). For WLCSP applications, the added cost to integrate all six process steps into one tool might not be justified based on the expected yields and throughputs. Wafers for WLCSP applications have relatively large spheres and have relatively few interconnects compared to flip chip applications. These larger spheres are placed in extremely high yields by the tool and the added expense of incorporating inspection and rework stations might not be justified (see Table 1 and Figure 5.).

Table 1. Process Steps for WLCSP Applications.

Process Step	Equipment
1. Flux Deposition	Spin Coater, SMT Printer, etc.
2. Sphere Transfer	Basic WLSST Tool
3. Reflow	Linear Oven
4. Wafer Clean	Solvent and/or DI Water Tools
5. Inspection	2D Scanner

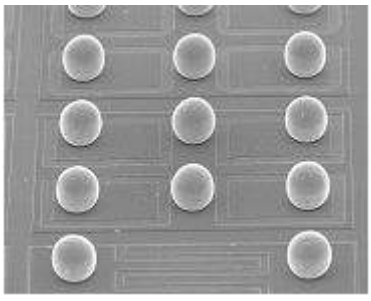

Figure 5. SEM Image of 300µm WLCSP Solder Bumps.

For flip chip applications, where high bump yields are an absolute requirement to give high die yields, integration of all these process steps may be critical to achieve this performance standard. It is common for high-end applications, such as microprocessors, to have hundreds of interconnects per die. Even small bump yield losses can translate into high die yield losses. The integration of the inspection and repair operations into the Wafer Level Solder Sphere Transfer tool makes sense for these flip chip applications (see Table 2 and Figure 6).

Table 2. Process Steps for Flip Chip Applications.

Process Step	Equipment
1. Fluxing Sphere Transfer 2D - Inspection Rework Hot Plate Reflow	Integrated WLSST Tool
2. Wafer Clean	Solvent and/or DI Water Tools

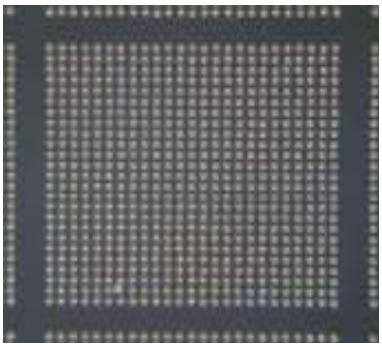

Figure 6. SEM Image of 100µm Flip Chip Bumps.

The uniformity of these bumps using the Wafer Level Solder Sphere Transfer process is singularly dependent on the size variation of the purchased spheres. The processes for making WLCSP and Flip Chip sized spheres are well established and suppliers can easily meet the uniformity specifications.

WLCSP PROCESSING STUDY

A program was undertaken to determine the manufacturability of combining e-Ni/Au plating with the Wafer Level Solder Sphere Transfer process for WLCSP applications. The goals of the study were to determine the throughput, yields, and reproducibility of the processes. Twenty five wafers with ~80,000 I/O pads were used as the test vehicle for this program (see Table 3 for wafer details).

Table 3. Test Wafer Properties

Wafer Size	200 mm
Wafer Thickness	360 µm
Die per wafer	3175
I/O per die	25
I/O on the wafer (bumped)	79,375
Pad Size	240 µm
Pad Pitch	500 µm
Pad Metallurgy	Al w/0.5%CU

The wafers were first plated with Ni/Au using an automated plating line. All twenty five wafers were plated as a single batch. This process took 55 minutes from start to finish. The plating line is capable of plating 50 wafers per batch and also capable of plating several batches concurrently. This brings the total throughput for plating to nearly 100 wafers per hour (see Table 4).

Table 4. Electroless Ni/Au Properties

Nickel Thickness	**5 µm**
Gold Thickness	**600 Å**
Phosphorous Content	**9 %**
Ni/Au Plating Time (per batch)	**55 min**
Throughput	**100 wafers/hr**
Plating Yield	**100 %**

The absolute nickel plating throughput values are partially dependent the physical characteristics of the wafer and the type of circuitry on the wafer. For example, if the wafer is thinned, the backside of the wafer may require backside coating to protect the wafer from plating on grind marks [13]. Another example of additional processing steps that might be required as part of the electroless plating process, is the requirement to plasma clean wafers which contain an organic passivation such as BCB or PI [14]. These additional steps will affect the throughput of the electroless plating process, depending on the throughput of these processes. In this study, the wafers did not require these additional processes.

Electroless Ni/Au plating yields are also highly dependent on the quality of the wafer. Any defects which are present on the I/O pads will result in defects in the plating process. The cleaning steps associated with the electroless Ni/Au plating process help eliminate any defects due to thin residues or contaminates. In addition, the die near the edge of the wafer are often incomplete and should be included in the exclusion zone for that device design.

After plating, the wafers were coated with a water soluble flux using an automated spin coater. The thickness of the flux is critical to ensure good placement and minimize any movement of the solder spheres during the solder sphere transfer operation. This thickness is controlled by flux viscosity and by the spinning speed (see Table 5).

Table 5. Flux Properties

Flux Type	**Water Soluble**
Fluxing Method	**Spin Coat**
Flux Thickness	**7 µm**
Process Time (25 wafers)	**25 min**
Throughput	**60 wafers/hr**

For this study, 300 µm preformed spheres were obtained from several suppliers. The performance of the spheres from each supplier was determined to be the comparable in a separate study (see Table 6).

Table 6. Solder Sphere Properties

Sphere Size	**300 µm**
Sphere Uniformity	**± 5 µm**
Solder Alloy	**SAC305**

The tooling plate which was used in the solder sphere transfer process was manufactured using a nickel plate up process. This tooling is very similar to a nickel plated stencil used in the surface mount industry. There are a large number of vendors who can now manufacture these stencils using electroforming techniques. The tolerances for these stencils is fairly loose due to the fact that the apertures size and stencil thickness do not need to accurately match the sphere size; as is the case in traditional solder sphere dropping techniques (see Table 7).

Table 7. WLSST Tooling Fixture Properties (stencil)

Aperture Size	**150 µm**
Stencil Thickness	**120 µm**
Stencil Material	**Electroformed (Ni Plated)**

The bumping throughput and yield for WLCSP applications is dependent on the accuracy of placing the spheres onto the wafer. Before processing the twenty five wafers though the Wafer Level Solder Sphere Transfer process, the accuracy and reproducibility of the solder sphere placement process was evaluated. A wafer was first coated with flux, and then placed into the WLSST tool and spheres transferred. The wafer was then visually inspected and the displacement of the spheres from the center of the pad (0, 0) was measured (see Figure 7 inset). This process was repeated a number of times to obtain statistics on sphere placement accuracy (see Table 8).

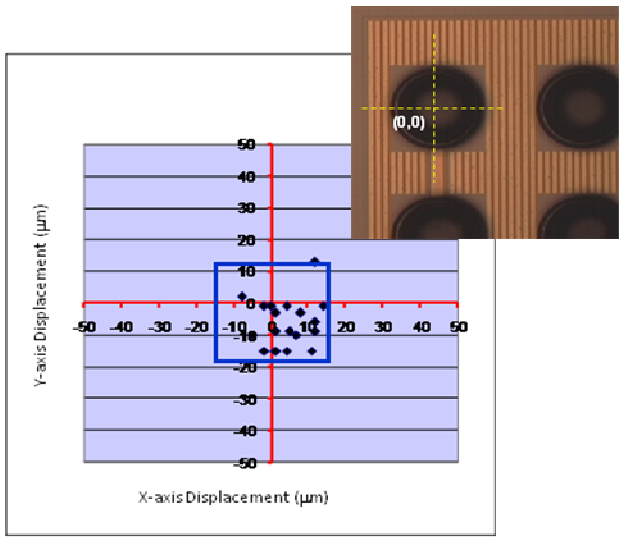

Figure 7. Graph of Sphere Placement Accuracy.

Table 8. Sphere Placement Statistics

	x	y
Minimum	**-8.00**	**-15.00**
Maximum	**14.00**	**13.00**
Average	**4.15**	**-6.65**
Std Deviation	**6.18**	**7.31**

The placement accuracy for transferring 300 μm spheres onto the 240 μm diameter pads was better than ±15μm (see Table 8). For WLCSP applications, this accuracy is more than adequate to ensure good wetting to a single I/O pad during reflow. For smaller spheres, this accuracy and reproducibility need to be tighter to ensure good yields. For these "flip chip" applications, the Wafer Level Solder Sphere Transfer tool is built with much higher tolerance mechanical and drive mechanisms.

For the throughput and yield study of the solder sphere transfer operation, the tool was preconfigured with the stencil tooling and the alignment confirmed and adjusted. At that point, the 25 wafers were continuously run through the Wafer Level Solder Sphere Transfer tool. The time required to process all 25 wafers was 50 minutes. This translates into a throughput value of 30 wafers per hour.

Table 9. WLSST Throughput Data

Transfer Time (25 Wafers)	**50 min**
Throughput	**30 wafers/hr**

The wafers (cassette of all 25) were then transferred over to a linear conduction oven for reflow. The wafers can be continuously processed through this tool with less than 30 sec per wafer separation and is therefore not considered to be a factor in the throughput of the integrated WLCSP process flow. After reflow, the wafers were cleaned in a batch process using ultrasonics and water rinsing. This too is not considered a limiting factor in determining the overall process throughput.

The wafers were optically inspected for sphere placement defects. This included, missing bumps, misshaped bumps, and bridged bumps. The yield numbers are reported in Tables 10 and 11. Yields of over 99.9% were observed for both sphere and die. For most WLCSP applications this is considered very high. If higher yields are still required, the addition of a solder ball jetting head can be added to replace any missing bumps prior to reflow. In this case, the optical alignment system is also used to scan the wafers for missing spheres.

Table 10. Sphere Yield

I/O placed with spheres (25 wafers)	I/O with Good Spheres after Transfer	Yield Loss	%Yield	ppm
1984375	**1984353**	**22 bumps**	**99.999%**	**9**

Table 11. Die Yield

Dies placed with spheres (25 wafers)	Good Dies after Sphere Transfer	Yield Loss	%Yield	ppm
79375	**79362**	**13 die**	**99.986%**	**139**

CONCLUSIONS

The combination of Electroless Nickel/Gold and Wafer Level Solder Sphere Transfer has been shown to be a viable process combination for WLCSP applications. Throughputs of greater than 25 wafers per hours have been demonstrated for all of the operations in the process flow. Bump and die yields of greater than 99.9% were realized.

The Wafer Level Solder Sphere Transfer process offers a good alternative to many of the other methods used to bump silicon wafers (stencil printing, electroplating, sphere drop, solder jetting, C4NP, and resist based template printing). Many of these other solder deposition processes have been practiced using varying degrees of automation. The Wafer Level Solder Sphere Transfer process is designed to run in either a semi-manual mode for prototyping, or highly automated for high volume applications. When coupled with an e-nickel UBM, the Wafer Level Solder Sphere Transfer technology can deliver one of the most versatile and lowest cost alternatives for WLCSP bumping. Continued innovation and volume implementation will make Wafer Level Solder Sphere Transfer a good alternative to the other bumping technologies.

In addition, the advantage of being able to deposit both Flip Chip and WLCSP sized bumps using the same equipment and same process flow, could help increase the implementation of wafer bumping (see Figure 8).

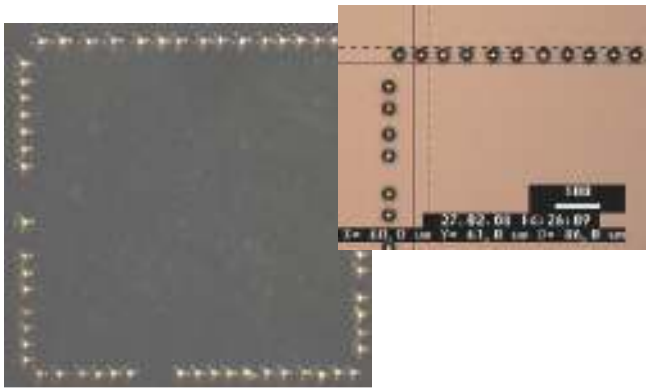

Figure 8. 60 μm Flip Chip Sized Bumps Transferred Using the Wafer Level Solder Sphere Transfer Tool.

This process has exceptional properties relative to bump size range (60-750 μm), yield (<10 ppm), and uniformity (<5 μm variation), and has the additional advantage of being able to deposit a wide variety of solder alloys, including high melting solders like AuSn or high-lead alloys, and ternary alloys like SnAgCu. The cost of the spheres is the main criteria that affects the cost of bumping. Because the spheres are priced on a per sphere basis, the bumping cost increases linearly as the number of I/Os increase on a wafer. The cost of these spheres is expected to drop as the implementation of the Wafer Level Solder Sphere Transfer process expands. Table 12 summarizes some for properties of the Wafer Level Solder Sphere Transfer process for both WLCSP and Flip Chip applications.

Table 12. Process Summary of the Wafer Level Solder Transfer Tool and Process

Category		WLCSP	Flip Chip
Wafer:	**Size**	**100-300 mm**	**100-300 mm**
Solder :	**Format** **Cost** **Type**	**Spheres** **$25-50 per million spheres** **All metal alloys (lead and lead free)**	**Spheres** **$35-50 per million spheres** **All metal alloys (lead and lead free)**
Bump Size :	**Range**	**200 – 750 μm**	**60 – 200 μm**
Sphere Placement:	**Accuracy**	**±15 μm**	**±5 μm**
Yield :	**Bump**	**< 25 ppm (wo/repair)**	**< 10 ppm (w/repair)**
Uniformity :	**Height**	**< 10 μm (sphere sizing)**	**< 5 μm variation (sphere sizing)**
Tooling :	**Type** **Cost (ea)**	**Nickel plated stencil** **$500 – 1000 (vendor dependent)**	**Nickel plated stencil** **$500 – 2000 (vendor dependent)**
Throughput :	**Wafers**	**25-45 wafers/hr**	**12-30 wafers/hr (w/repair)**

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